CLAIMS

What is claimed is:

1. An interconnect adapted for use with a pixel layer of a pixel web, comprising:

an interconnect substrate including a plurality of conductive leads;

a plurality of contact vias formed on and extending from said interconnect substrate, said plurality of contact vias being formed in a predetermined pattern on said interconnect substrate and being in electrical communication with said plurality of conductive leads of said interconnect substrate; and

a patterned spacer of a thickness substantially equal to a height of said plurality of contact vias, said patterned spacer including a plurality of through-holes also formed according to said predetermined pattern and having a dimension substantially equal to a dimension of said plurality of contact vias;

wherein said interconnect substrate and said patterned spacer are capable of being assembled onto said pixel layer of said pixel web, with said patterned spacer being in a middle position and said plurality of contact vias extending through said plurality of through-holes of said patterned spacer to contact corresponding cathode portions on said pixel layer.

2. The interconnect of claim 1, wherein said patterned spacer is formed of a dielectric material.

3. The interconnect of claim 1, wherein said patterned spacer is formed of an insulator material.

4. The interconnect of claim 1, wherein said interconnect substrate further comprises at least one driver formed as part of said interconnect substrate and providing an electrical drive current to an associated contact via.

5. The interconnect of claim 1, wherein multiple contact vias are capable of being in contact with a cathode portion of said pixel layer.

6. The interconnect of claim 1, wherein multiple contact vias are capable of being in contact with a cathode portion of said pixel layer, and wherein said multiple contact vias are spaced according to a predetermined distribution pattern.

7. The interconnect of claim 1, wherein said patterned spacer is formed on said pixel layer.

8. The interconnect of claim 1, wherein said patterned spacer is formed on said interconnect substrate.

9. The interconnect of claim 1, wherein a plurality of cathodes are formed in columns on said pixel layer, with a cathode of said plurality of cathodes comprising a plurality of individual cathode portions.

10. An interconnect adapted for use with a pixel layer of a pixel web, comprising:

a plurality of cathodes formed in columns on said pixel layer, with a cathode of said plurality of cathodes comprising a plurality of individual cathode portions;

an interconnect substrate including a plurality of conductive leads;

a plurality of contact vias formed on and extending from said interconnect substrate, said plurality of contact vias being formed in a predetermined pattern on said interconnect substrate and being in electrical communication with said plurality of conductive leads of said interconnect substrate;

at least one driver formed in said interconnect substrate, with said at least one driver providing an electrical drive current to an associated contact via; and

a patterned spacer of a thickness substantially equal to a height of said plurality of contact vias, said patterned spacer including a plurality of through-holes also formed according to said predetermined pattern and having a dimension substantially equal to a dimension of said plurality of contact vias;

wherein said interconnect substrate and said patterned spacer are capable of being assembled onto said pixel layer of said pixel web, with said patterned spacer being in a middle position and said plurality of contact vias extending through said plurality of through-holes of said patterned spacer to contact corresponding cathode portions on said pixel layer.

11. The interconnect of claim 10, wherein multiple contact vias are capable of being in contact with a cathode portion of said pixel layer.

12. The interconnect of claim 10, wherein multiple contact vias are capable of being in contact with a cathode portion of said pixel layer, and wherein said multiple contact vias are spaced according to a predetermined distribution pattern.

13. The interconnect of claim 10, wherein said patterned spacer is formed on said pixel layer.

14. The interconnect of claim 10, wherein said patterned spacer is formed on said interconnect substrate.

15. A method of forming a plurality of electrical connections to a pixel layer of a pixel web, comprising the steps of:

providing an interconnect substrate, said interconnect substrate including a non-conducting face and a plurality of exposed electrical contacts formed in a predetermined pattern; and

placing said interconnect substrate in contact with said pixel layer, with said plurality of exposed electrical contacts of said interconnect substrate contacting predetermined regions of said pixel layer;

wherein a plurality of conductive leads may extend from substantially any region of a backside of said pixel layer of said pixel web.

16. The method of claim 15, wherein said providing step further comprises the steps of:

forming said interconnect substrate having said plurality of conductive leads therein;

depositing a spacer material onto said pixel layer;

forming a plurality of holes in said spacer material according to said predetermined pattern, with said holes being positioned substantially over cathode portions of said pixel layer and substantially corresponding to said plurality of conductive leads of said interconnect substrate; and

depositing a conductive material in said plurality of holes to form a plurality of contact vias, with said plurality of contact vias capable of being in electrical communication with said plurality of conductive leads.

17. The method of claim 16, wherein multiple contact vias of said plurality of contact vias contact an individual cathode portion of said pixel layer.

18. The method of claim 15, wherein said providing step further comprises forming a plurality of drivers on said interconnect substrate.

19. The method of claim 15, further comprising a step of segmenting a cathode of said pixel layer into a plurality of individual cathode portions, with a cathode portion of said plurality of individual cathode portions being contacted by at least one exposed electrical contact of said interconnect substrate.